IN THE CLAIMS

Please amend the claims by canceling claims 38-64. No other amendments are made to the claims. Original claims 1-37 are reproduced below for the convenience of the Examiner.

1. (Original) An integrated circuit (IC) package substrate comprising a plurality of conductors within an IC mounting region, each conductor to be electrically coupled to a respective terminal of an IC, and at least one capacitor within the IC mounting region.

2. (Original) The IC package substrate recited in claim 1, wherein the at least one capacitor is electrically coupled to at least one conductor.

3. (Original) The IC package substrate recited in claim 2, wherein the at least one capacitor is mounted atop the at least one conductor.

4. (Original) The IC package substrate recited in claim 3, wherein the at least one capacitor is a capacitor array comprising two surfaces, each having a plurality of terminals of first and second polarity types.

5. (Original) The IC package substrate recited in claim 4, wherein the plurality of terminals of the capacitor array are disposed over substantially the entire surfaces.

6. (Original) The IC package substrate recited in claim 2, wherein the at least one capacitor is mounted beside the at least one conductor.

7. (Original) The IC package substrate recited in claim 1, wherein the conductors include at least one conductive bar having a height and a width, the height exceeding the width, and wherein the at least one capacitor is mounted beside and in electrical contact with the at least one conductive bar.

8. (Original) The IC package substrate recited in claim 1, wherein the plurality of conductors are substantially parallel to one another.

9. (Original) The IC package substrate recited in claim 8, wherein the at least one capacitor is non-orthogonally mounted atop the at least one conductor.

10. (Original) The IC package substrate recited in claim 1 and comprising a plurality of capacitors distributed substantially throughout the IC mounting region, each capacitor being in electrical contact with at least one of the conductors.

11. (Original) The IC package substrate recited in claim 10, wherein the plurality of capacitors comprises a plurality of sets of capacitors, each set comprising one or more capacitors aligned substantially end-to-end.

12. (Original) The IC package substrate recited in claim 1, wherein the conductors include pads.

13. (Original) An integrated circuit (IC) comprising:

a plurality of conductive bars on a surface of the IC, each conductive bar to be electrically coupled to a respective terminal of an IC package substrate; and

at least one capacitor having terminals coupled to at least two of the conductive bars.

14. (Original) The IC recited in claim 13, wherein the conductive bars have a height and a width, the height exceeding the width.

15. (Original) The IC recited in claim 14, wherein the at least one capacitor is mounted beside and in electrical contact with the at least two conductive bars.

16. (Original) An integrated circuit (IC) package comprising:

a substrate having a plurality of conductors within an IC mounting region;

at least one capacitor within the IC mounting region and electrically coupled to at least one of the conductors; and

an IC electrically coupled to the plurality of conductors.

17. (Original) The IC package recited in claim 16, wherein the at least one capacitor is electrically coupled to first and second conductors of the plurality of conductors, and wherein the first conductor is to couple to a first potential, and the second conductor is to couple to a second potential.

18. (Original) The IC package recited in claim 16, wherein the at least one capacitor is mounted atop the at least one conductor.

19. (Original) The IC package recited in claim 18, wherein the at least one capacitor is mounted atop two conductors.

20. (Original) The IC package recited in claim 18, wherein the at least one capacitor is an capacitor array having two surfaces, each having a plurality of terminals of first and second polarity types.

21. (Original) The IC package recited in claim 20, wherein the plurality of terminals are disposed over substantially the entire surfaces.

22. (Original) The IC package recited in claim 16, wherein the at least one capacitor is mounted beside the at least one conductor.

23. (Original) The IC package recited in claim 16, wherein the at least one capacitor is mounted between two conductors.

24. (Original) The IC package recited in claim 16, wherein the at least one capacitor has a top, a bottom, and a pair of opposing sides, and wherein the at least one capacitor is from the group comprising a capacitor having terminals on its top and bottom, a capacitor having terminals on its opposing sides, and a capacitor having terminals on its top, bottom, and opposing sides.

25. (Original) The IC package recited in claim 16, wherein the conductors include at least one conductive bar having a height and a width, the height exceeding the width, and wherein the at least one capacitor is mounted beside and in electrical contact with the at least one conductive bar.

26. (Original) The IC package recited in claim 16, wherein the plurality of conductors are substantially parallel to one another.

27. (Original) The IC package recited in claim 26, wherein the at least one capacitor is non-orthogonally mounted atop the at least one conductor.

28. (Original) The IC package recited in claim 16 and comprising a plurality of capacitors distributed substantially throughout the IC mounting region, each capacitor being in electrical contact with at least one of the conductors.

29. (Original) The IC package recited in claim 28, wherein the plurality of capacitors comprises a plurality of sets of capacitors, each set comprising one or more capacitors aligned substantially end-to-end.

30. (Original) The IC package recited in claim 16, wherein the conductors include pads.

31. (Original) An electronic assembly comprising:

a printed circuit board (PCB); and

an integrated circuit (IC) package coupled to the PCB and including

a substrate having a plurality of conductors within an IC mounting region;

at least one capacitor within the IC mounting region and electrically coupled to at least one of the conductors; and

an IC electrically coupled to the plurality of conductors.

32. (Original) The electronic assembly recited in claim 31, wherein the at least one capacitor is electrically coupled to two of the conductors, one conductor to couple to a first potential, the other conductor to couple to a second potential.

33. (Original) The electronic assembly recited in claim 31, wherein the at least one capacitor is mounted atop the at least one conductor.

34. (Original) The electronic assembly recited in claim 31, wherein the at least one capacitor is mounted beside the at least one conductor.

35. (Original) An electronic system comprising:

a bus coupling components in the electronic system;

a display coupled to the bus;

external memory coupled to the bus; and

a processor coupled to the bus and comprising an electronic assembly including:

a printed circuit board (PCB); and

an integrated circuit (IC) package coupled to the PCB and including

a substrate having a plurality of conductors within an IC mounting region;

at least one capacitor within the IC mounting region and electrically coupled to at least one of the conductors; and

an IC electrically coupled to the plurality of conductors.

36. (Original) The electronic system recited in claim 35, wherein the at least one capacitor is mounted atop the at least one conductor.

37. (Original) The electronic system recited in claim 35, wherein the at least one capacitor is mounted beside the at least one conductor.

Claims 38-64 (Canceled)